VIA HOLE DEFINING PROCESS PERFORMED IN ONE CHAMBER

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 91100849, filed January 21, 2002.

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a via process in a semiconductor process. More particularly, the present invention relates to a via hole defining process performed in one chamber.

Description of Related Art

[0002] Refer to FIG. 1A~1C, FIG. 1A~1C illustrate a conventional via hole defining process in a multi-layer interconnection process of a semiconductor device. This via hole defining process is designed to enhance the step coverage effect of a conductive layer filled into the via hole.

[0003] Refer to FIG. 1A, a dielectric layer 102 is formed on a substrate 100 and then a patterned photoresist layer 104 is formed on the dielectric layer 102. The patterned photoresist layer 104 has an opening 106 therein.

[0004] Refer to FIG. 1B, an isotropic etching 108 is performed to the dielectric layer 102 in a wet etching chamber to form a cavity 110 therein, using the patterned photoresist layer 104 as a mask.

[0005] Refer to FIG. 1C, by using the patterned photoresist layer 104 as a mask, an anisotropic etching 112 is conducted to form a via hole 114 in the dielectric layer 102 in

a dry etching chamber.

[0006] Since the conventional via hole defining process includes two different types of etching steps, at least two etching chambers are required. Therefore, the conventional via hole defining process has a higher time-cost and greater risks of wafer damage from delivering steps between different chambers.

SUMMARY OF THE INVENTION

[0007] Accordingly, this invention provides a via hole defining process completed in a single chamber in order to save the process time and lower the risks of wafer damage.

[0008] The via hole defining process of this invention comprises the following steps. A substrate with a dielectric layer thereon is provided and then a patterned mask layer having an opening is formed on the dielectric layer. An anisotropic etching process is then conducted to form a via hole in the dielectric layer within an etching chamber by using the patterned mask layer as a mask. A portion of the patterned mask layer around the via hole is then removed by a dry-etching method, such as oxygen (O_2) treatment, to broaden the opening in the patterned mask layer in the same etching chamber, while the profile of the via hole is retained. Another anisotropic etching process is then conducted to remove a portion of the dielectric layer exposed by the remaining mask layer around the upper portion of the via hole.

[0009] In the present invention, a dry-etching method is utilized to broaden the opening in the patterned mask layer, and then an anisotropic etching is performed to broaden the upper portion of the via hole. Therefore, the via hole defining process of the present invention can be completed in a single chamber to save the process time. Moreover, because the via hole defining process is completed in a single chamber, the

wafer damage caused by delivering steps between different chambers can be avoided.

[0010] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0012] FIG. 1A~1C illustrate the cross-sectional views of the process flow of a conventional via hole defining process; and

[0013] FIG. 2A~2D illustrate the cross-sectional views of the process flow of a via hole defining process completed in one etching chamber according to a preferred embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0014] The via hole defining process according to one preferred embodiment of this invention will be described hereinafter by referring to FIG. 2A~2D. However, this invention can also be used in other multi-layer interconnection processes including a contact hole defining process.

[0015] Refer to FIG. 2A~2D, FIG. 2A~2D illustrate the cross-sectional views of the process flow of a via hole defining process completed in one etching chamber according to the preferred embodiment of this invention.

[0016] Refer to FIG. 2A, a dielectric layer 202 is formed on a substrate 200. A patterned mask layer 204, such as a patterned photoresist layer, is formed on the dielectric layer 202. The patterned mask layer 204 has an opening 206 therein.

[0017] Refer to FIG. 2B, the dielectric layer 202 is then subjected to a first anisotropic etching 208 within an etching chamber (not sown) to form a via hole 210 therein by using the patterned mask layer 204 as a mask. The etching chamber can be a clean mode etching chamber, while a reaction gas used in the first anisotropic etching process comprises, for example, fluorohydrocarbons ($C_xH_yF_z$) and may further comprise carbon monoxide (CO), oxygen (O_2), or argon (Ar).

[0018] Refer to FIG. 2C, an oxygen (O_2) treatment is performed in the same etching chamber to remove a portion of the mask layer 204 around the via hole 210, so as to create a larger opening 206a in the mask layer 204a. A bottom power and a top power used in the oxygen plasma treatment are respectively of a range, for example, from 0.1W to 50W and from 500W to 2000W.

[0019] Since the O_2 treatment with a low power is used to remove a portion of the patterned mask layer 204, the profile of the via hole 210 can be substantially maintained. However, to minimize the degree of deformation of the via hole 210, the dielectric layer 202 preferably comprises an inorganic oxide material, such as silicon oxide. On the contrary, in order to be removed by the oxygen plasma, the patterned mask layer 204 may comprise a photoresist, a spin-on polymer (SOP), or an organic low-K material.

[0020] Refer to FIG. 2D, the dielectric layer 202 is then subjected to a second anisotropic etching 208 within the same etching chamber to remove a portion of the dielectric layer 202 that is exposed by the remaining mask layer 204a. The upper

portion of the via hole 210 is thereby broadened and becomes a larger opening 216 in the dielectric layer 202.

[0021] In the subsequent process (not shown), the patterned mask layer 204a is removed and then a conductive layer is formed over the substrate 200 to fill the via hole 210 and the opening 216. A chemical mechanical polishing (CMP) process is conducted later to form a via plug in the via hole and in the opening.

[0022] As described in the preferred embodiment of this invention, an O_2 treatment is utilized to broaden the opening in the patterned mask layer and then an anisotropic etching is performed to broaden the upper portion of the via hole. Therefore, the via hole defining process can be completed in a single chamber, thus saving the process time. Moreover, because the via hole defining process is completed in a single chamber, the wafer damage caused by delivering steps between different chambers can be avoided.

[0023] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.